the metal-containing gate conductor, and the upper surface of both the gate dielectric and the high-k gate dielectric that is present at the gate corners.

[0019] In yet another embodiment of the present invention, the gate spacer is a low-k dielectric material (dielectric constant of less than 4). In a further embodiment, the gate spacer includes a void present in the interior thereof which lowers the effective dielectric constant of the gate spacer.

[0020] In an even further embodiment of the present invention, the high-k gate dielectric present at the gate corners is strengthened by introducing oxygen and/or nitrogen into the material which is present at the gate corners.

[0021] In addition to the general semiconductor structure mentioned above, the present invention also provides a semiconductor structure that comprises:

[0022] at least one metal oxide semiconductor field effect transistor (MOSFET) located on a surface of a semiconductor substrate, said at least one MOSFET comprising a gate stack including, from bottom to top, a high-k gate dielectric and a metal-containing gate conductor, said metal-containing gate conductor having gate corners located at a base segment of the metal-containing gate conductor, wherein said metal-containing gate conductor has vertical sidewalls devoid of said high-k gate dielectric except at said gate corners, said high-k gate dielectric at said gate corners has increased bonding as compared to said high-k gate dielectric that is located directly beneath said metal-containing gate conductor;

[0023] a gate dielectric laterally abutting said high-k gate dielectric present at said gate corners; and

[0024] a gate spacer laterally abutting said metal-containing gate conductor and located upon an upper surface of both the gate dielectric and the high-k gate dielectric that is present at the gate corners.

[0025] In another embodiment, the present invention provides a semiconductor structure that comprises:

[0026] at least one metal oxide semiconductor field effect transistor (MOSFET) located on a surface of a semiconductor substrate, said at least one MOSFET comprising a gate stack including, from bottom to top, a high-k gate dielectric and a metal-containing gate conductor, said metal-containing gate conductor having gate corners located at a base segment of the metal-containing gate conductor, wherein said metal containing gate conductor has vertical sidewalls devoid of said high-k gate dielectric except at said gate corners;

[0027] a gate dielectric laterally abutting said high-k gate dielectric present at said gate corners; and

[0028] a low-k gate spacer that includes voids in the interior thereof laterally abutting said metal-containing gate conductor and located upon an upper surface of both the gate dielectric and the high-k gate dielectric that is present at the gate corners.

[0029] In addition to the semiconductor structure described above, the present invention also provides a method of fabricating such a semiconductor structure. In general terms, the method of the present invention includes:

[0030] providing a structure including a sacrificial gate conductor and a gate dielectric located on a semiconductor substrate, said structure further including an interlevel dielectric located on said semiconductor substrate and separated from said sacrificial gate by a sacrificial spacer;

[0031] removing the sacrificial gate and a portion of the gate dielectric that is not protected by the sacrificial spacer to form an opening that exposes a surface of the semiconductor substrate;

[0032] forming a U-shaped high-k gate dielectric and a metal-containing gate conductor inside the opening;

[0033] removing the sacrificial spacer to expose a portion of the U-shaped high-k gate dielectric that laterally abuts sidewalls of the metal-containing gate conductor;

[0034] removing substantially all of the exposed portion of the high-k gate dielectric that laterally abuts the sidewalls of the metal-containing gate conductor from the gate sidewalls; and

[0035] forming a gate spacer in an area that previously included the sacrificial spacer and a portion of the U-shaped high-k gate dielectric.

BRIEF DESCRIPTION OF THE DRAWINGS

[0036] FIG. **1** is a pictorial representation (through a cross sectional view) illustrating a prior art high-k gate dielectric/metal conductor MOSFET that was fabricated utilizing a conventional gate replacement process.

[0037] FIGS. **2**A, **2**B and **2**C are pictorial representations (through cross sectional views) illustrating high-k gate dielectric/metal-containing conductor MOSFETs in accordance with three embodiments of the present invention.

[0038] FIGS. **3**A-**3**H are pictorial representations (through cross sectional views) illustrating the basic processing steps that can be used in fabricating the structures shown in FIGS. **2**A-**2**C.

DETAILED DESCRIPTION OF THE INVENTION

[0039] The present invention which provides a high-k gate dielectric/metal-containing MOSFET having at least reduced contact-to-gate conductor parasitic capacitance and a method of fabricating the same, will now be described in greater detail by referring to the following description and drawings that accompany the present application. It is noted that the drawings of the present application are provided for illustrative purposes only and, as such, the drawings are not drawn to scale.

[0040] In the following description, numerous specific details are set forth, such as particular structures, components, materials, dimensions, processing steps and techniques, in order to provide a thorough understanding of the present invention. However, it will be appreciated by one of ordinary skill in the art that the invention may be practiced without these specific details. In other instances, well-known structures or processing steps have not been described in detail in order to avoid obscuring the invention.

[0041] It will be understood that when an element as a layer, region or substrate is referred to as being "on" or "over" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or "directly over" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "beneath" or "under" another element, it can be directly beneath or under the other element, or intervening elements may be present. In contrast, when an element is referred to as being "directly beneath" or "directly under" another element, there are no intervening elements present.

[0042] Also, it is observed that although the following description and drawings show the presence of a single high-k gate dielectric/metal-containing conductor MOSFET, the present invention is not limited to the same. Instead, a plurality of high-k gate dielectric/metal-containing conductor